



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,157	02/27/2002	Kazuhiko Hanawa	381AS/50958	8695

7590

11/30/2005

CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER

ISMAIL, SHAWKI SAJJ

ART UNIT

PAPER NUMBER

2155

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/083,157

Applicant(s)

HANAWA, KAZUHIKO

Examiner

Shawki S. Ismail

Art Unit

2155

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the application filed on February 27, 2002.
Claims 1-12 are presented for examination.
Applicant's claim for foreign priority is acknowledged.
References in applicant's IDS form 1449 have been considered.

Claim Rejections - 35 USC §102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 12-24, and 29-34, are rejected under 35 U.S.C. 102(e) as being anticipated by **Kennedy** U.S. Patent No. **5,659,748**.
4. As to claims 1, Kennedy teaches a signal processing apparatus, comprising:
first computing means and second computing means operating independent of each other (col. 2, lines 6-19 and col. 3, lines 23-45, default boot CPU and alternate CPU); and
interface means interconnecting said first computing means and said second computing means (col. 2, lines 6-19, and col. 3, lines 23-45, see Fig. 1, an interface connects both the CPU's),
wherein upon power-up of said signal processing apparatus, said first computing means transfers data to said second computing means by way of said interface means,

Art Unit: 2155

whereupon signal processing in an ordinary operation mode is executed (col. 2, lines 6-19, upon power up, if default boot CPU fails control transfers automatically to alternate CPU).

5. As to claims 2, Kennedy teaches a signal processing apparatus according to claim 1,

wherein said first computing means transfers the data required by said second computing means (see abstract, the system automatically transfers default system initialization operations from a default processor to a first alternative processor).

6. As to claims 3, Kennedy teaches a signal processing apparatus according to claim 1, further comprising:

data rewritable nonvolatile memory means (col. 5, lines 1-24),

said nonvolatile memory means having a program memory map corresponding to said first computing means (col. 5, lines 1-24),

wherein a run start address of said second computing means, a program data size and program data therefor are arrayed in a parameter table area of said program memory map corresponding to said first computing unit (col. 7, lines 24-33).

7. As to claims 4, Kennedy teaches a signal processing apparatus according to claim 1,

wherein said interface means includes a serial interface and general-purpose signaling means (col. 3, lines 55-66).

8. As to claims 5, Kennedy teaches a signal processing apparatus according to claim 4,

wherein said first and second computing means are so arranged that upon power-up of said signal processing apparatus, said first computing means firstly transfers data of a predetermined unitary amount to said second computing means via said serial interface, while said second computing means inverts polarity of said general-purpose signaling means after lapse of a predetermined time since the end of the first data transfer, and when said first computing means starts again the data transfer, said second computing means inverts again the polarity of said general-purpose signaling means, to thereby carry out the data transfer upon power-up of said signal processing apparatus through repetition of the data transfer and the polarity inversion of said general-purpose signaling means, whereupon signal processing in an ordinary operation mode is executed (col. 3, lines 55-66 and col. 4, lines 26-47)

9. As to claims 6, Kennedy teaches a signal processing apparatus according to claim 1, further comprising:

read-only memory means incorporated in said second computing means (col. 5, lines 25-35); and

volatile memory means incorporated in said second computing means or connected thereto by way of an address bus and a data bus (col. 5, lines 25-35).

10. As to claims 7-12, they do not teach or define any new limitations above claims 1-6 and therefore they are rejected for similar reasons.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawki S Ismail whose telephone number is 571-272-3985. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawki Ismail
Patent Examiner
November 28, 2005



SALEH NAJJAR
SUPERVISORY PATENT EXAMINER